**North South University**

Department of Computer Science and Engineering

Quiz-4, Section – 3, Summer’17

Course No: **CSE 332** Course Title: **Computer Organization and Design**

Time: 20 min Full Marks: 15

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1. | Assume time for different stages is as follows:  80ps for register read or write  100ps for inctr. Fetch  150 ps for other stages   * fill up the following table. * Identify the cock cycle time(Tc) for the pipelined version and non pipelined version * How faster is the pipelined version in compared to the non pipelined version  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **Instruction** | **Instr. Fetch** | **Instr. Decode** | **EX** | **Mem** | **Write Back** | **Total Time** | | **lw** |  |  |  |  |  |  | | **addi** |  |  |  |  |  |  | | **beq** |  |  |  |  |  |  | |  |  |  |  |  |  |  | | 9 |
| 2. | Consider the following codes for a MIPS 5 stage pipelined architecture and answer the question   * Locate the hazards? * How many clock cycles would it require for performing correctly (after solving hazards). * Please minimize the number of clock cycles if possible (by reordering).   lw $t1, 0($t0)  add $t1, $t2, $t4  sub $t4, $t1, $t3  add $t5, $t1, $t2  sw $t3, 8($t0)  lw $t3, 8($t0) | 6 |